Jaidev P. Patwardhan

Curriculum Vitae

Last Updated: June 2006
Most recent version available at: http://www.cs.duke.edu/~jaidev

100 Erlwood Way, #202
Durham, NC 27704

Home Phone: 919-321-0348
Cell Phone: 919-949-2691
Email: jaidev@cs.duke.edu

Education

- PhD in Computer Science, Duke University (Expected Graduation Date: Summer 2006)
  Advisor: Prof. Alvin R. Lebeck
  Thesis Topic: Architectures for Nanoscale Devices
- M.S in Computer Science, Duke University (May 2002)
  Advisor: Prof. Alvin R. Lebeck
  Project Title: Register File Management for Kilo Instruction Window Processors
- B.E in Computer Engineering, V.J.T.I, Mumbai, India (May 2000)

Interests

My primary area of interest is computer architecture, encompassing processor to platform architectures. I am interested in designing resilient, high performance parallel and general-purpose architectures. I am also interested in the application of performance analysis and debugging techniques at various levels of the platform (microarchitecture, chipset, application and systems software) to improve system performance.

Work Experience

- Research Assistant: Department of Computer Science, Duke University
  Supervisor: Prof. Alvin R. Lebeck.
  Project: Architectures for Emerging Nanoscale Devices (2003-Present)
  My thesis explores the impact of emerging nanoscale technologies on architecture design through the design and evaluation of two high-performance, defect-tolerant architectures. This includes developing and implementing the circuit model (VHDL), the microarchitecture, instruction set architecture and system architecture, as well as creating simulation infrastructure for both architectures. [FNANO 2004][NANOTECHNOLOGY 2004][NANOARCH 2005] [JETC 2006][NANOARCH 2006][ASPLOS 2006]
  Project: Communication Oriented Architectures (2002-2003)
  The goal of this project was to evaluate the benefits of hardware protocol offload for improving the performance of web workloads. I evaluated TCP/IP processing overheads in static, dynamic and multi-tier commercial web-workloads using performance analysis and instrumentation tools. This was an extension of work done as a summer intern at Intel. [ISPASS 2004]
  Project: Register File Design for Kilo-Instruction Window Processors (2001-2002)
  I examined physical organizations for low latency, high capacity register files to support large instruction windows. This included modeling the register files in an architectural simulator, as well as at the circuit level.
- Graduate Technical Intern: Intel Corp, Hillsboro, Oregon (May 2002 – August 2002)

Mentor(s): Douglas Carmean, Herbert Hum
Group: Desktop Processor Group (DPG-CPU Arch)
Project: Support for Accelerated Network Processing
The goal of this project was to evaluate the utility of increased hardware support for TCP/IP processing. I analyzed TCP/IP processing overheads in a CPU for a simple communication workload using performance analysis and instrumentation tools. My work provided useful feedback in improving the performance analysis tool. [ISPASS 2003]

- Teaching Assistant: Department of Computer Science, Duke University
  Course: "Computer Organization, Design and Programming" (Fall '01, Spring '02)

Publications

Journal

- "NANA: A Nanoscale Active Network Architecture", J. P. Patwardhan, C. L. Dwyer, A. R. Lebeck, D. J. Sorin. *ACM Journal on Emerging Technologies in Computing Systems)* Vol. 2, No. 1, Pages 1-30, January 2006.
- "Design Tools for Self-Assembling Nanoscale Technology", C.L. Dwyer, V. Johri, J. P. Patwardhan, A. R. Lebeck, D. J. Sorin. *Institute of Physics, Nanotechnology* 15(2004)

Conference

- "Self-Assembled Networks: Control vs. Complexity", J. P. Patwardhan, C. L. Dwyer, A. R. Lebeck. In submission, NANONETS 2006
- "A Defect Tolerant Self-Organizing Nanoscale SIMD Architecture", J. P. Patwardhan, V. Johri, C. L. Dwyer, A. R. Lebeck. To appear, ASPLOS 2006
- "Circuit and System Architecture for DNA-Guided Self-Assembly of Nanoelectronics", J. P. Patwardhan, C. L. Dwyer, A. R. Lebeck and D. J. Sorin. Invited paper in the *Proceedings of the Foundations of Nanoscience: Self-Assembled Architectures and Devices* (FNANO), 2004.
- "Communications Breakdown: Analyzing CPU Usage in Commercial Web Workloads", J. P. Patwardhan, A. R. Lebeck and D. J. Sorin. Proceedings of the *International Symposium on Performance Analysis of Systems and Software* (ISPASS), 2004.
- "TCP Performance Re-visited", A. Foong, T. Huff, H. Hum, J. P. Patwardhan, G. Regnier. *Proceedings of the International Symposium on Performance Analysis of Systems and Software* (ISPASS), 2003.
- "A Large, Fast Instruction Window for Tolerating Cache Misses", A. R. Lebeck, J. Koppnnalil, T. Li, J. P. Patwardhan and E. Rotenberg. *Proceedings of the International Symposium on Computer Architecture* (ISCA), 2002.

Workshop

- "Design and Evaluation of Fail-Stop Self-Assembled Nanoscale Processing Elements" J. P. Patwardhan, C. L. Dwyer and A. R. Lebeck. To appear, NANOARCH 2006
- "Evaluating the Connectivity of Self-Assembled Networks of Nano-scale Processing Elements", J. P. Patwardhan, C. L. Dwyer, A. R. Lebeck, D. J. Sorin. In *Proceedings of the IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH)*, Palm Springs, CA , May 2005.

- "Exploring the Benefits of a Continuous Consistency Model for Wireless Web Portals", Jagadeeswaran Rajendiran, Jaidev Patwardhan, Vijay Abhijit, Rahul Lakhotia, and Amin Vahdat. *Proceedings of the IEEE Workshop on Internet Applications*, San Jose, CA , July 2001.

Refereed Posters

- "SSA: A Self-Organizing SIMD Architecture", J. P. Patwardhan, C.Dwyer, and A. R. Lebeck. In *Proceedings of the Workshop on Edge Computing Using New Commodity Architectures (EDGE)*, 2006.
- "NANA: A Nanoscale Active Network Architecture", J. P. Patwardhan, C.Dwyer, A. R. Lebeck, and D. J. Sorin. In *Proceedings of the Foundations of Nanoscience: Self-Assembled Architectures and Devices* (FNANO), 2004.
- "CAD Support for DNA-Guided Self-Assembly of Nano-electronics", C. Dwyer, V.Johri, M. Cheung, J.P.Patwardhan, A.R.Lebeck, D.J.Sorin. In *Proceedings of the Foundations of Nanoscience: Self-Assembled Architectures and Devices* (FNANO), 2004.

Relevant Skills and Course Work

- *Languages*: C, C++ (including VC++), Java, Perl, VHDL.
- *Platforms*: Linux, UNIX, and Windows.
- *Specific Technologies/packages*: Mentor Graphics CAD tools, HSPICE, SimpleScalar Toolset.
- Trained on Scanning Electron Microscope, E-Beam Lithography, E-Beam Evaporator.
- *Graduate Courses*: Advanced Computer Architecture, Parallel Computer Architecture, Advanced Digital System Design, Full Custom VLSI Design, Ubiquitous Computing, Computer Networks & Distributed Systems, Operating Systems, Mathematical Methods of Systems Analysis, Design and Analysis of Algorithms.

Departmental and Professional Service

- Reviewer: FAST 2002, ICPADS 2004, SIGMETRICS 2005, ISPASS 2006, ICCD 2006
- Co-Chair: Graduate Student Faculty Search Committee, 2005
- Member: Graduate Student Faculty Search Committee, 2001-04
- Member: Graduate Student Recruitment Committee, 2001-04
- Member: Space Allocation Committee, 2002-05

Honors & Awards

- Recipient of a Graduate Fellowship from the Department of Computer Science, Duke University
- Recipient of "Outstanding Graduate Teaching Assistant Award" from Department of Computer Science, Duke University. (2002)

Professional Affiliations

- Student Member, Association of Computing Machinery (ACM)
- Student Member, Institute of Electrical and Electronic Engineers (IEEE)

References: Available on request